



**A One Week Workshop on
Parallel Programming for Parallel and Distributed Architectures
06 to 10 December 2021, Online Mode
Organized by IIITDM Kancheepuram, Chennai-600 127**

Venue	Online Mode
Objective	This workshop aims to provide the basics of modern processor architecture and serial optimization techniques that can effectively exploit the architectural features for scientific computing. Critical issues in data movement and issues in high performance computing are discussed. The use of parallel processing in shared, nonuniform access, and distributed memories is discussed. In addition the popular programming styles of OpenMP, MPI and mixed programming are highlighted. Hands on sessions will be conducted on the IIITDM Cluster Computer.
Topics to be Covered	<ul style="list-style-type: none">• Introduction to Parallel Architectures and High Performance Computing.• Modern Processor Architecture scope of Parallel programming.• Profiling the Serial Code – Functional, Line based and Hardware Performance Counter.• Data Access and Machine Balance. Computational Performance vs Memory Bandwidth.• Parallel Computer Architecture and limitations.• Parallelization fundamentals.• Shared Memory Parallel Programming with OpenMP.• Distributed Memory Parallel Programming with MPI.• Programming GPGPU Architectures with CUDA.
Target Audience	Faculty/Scientists/Industry Persons/Researchers/M. Tech/MCA/BCA/BSc and B. Tech Students working in the area of Parallel Programming or High Performance Computing.
Prerequisite	Participant should have the basic working knowledge of C Programming, and Computer.
Registration Details	Registration Link: https://docs.google.com/forms/d/e/1FAIpQLSfOyHc_50kb9slc4daF-OUa1GGqVt6ZslcCicAQsE-rqNkZEg/viewform
Registration Fees	Faculty/Scientists/Industry or R&D Persons/Researchers/M. Tech/MCA/BCA/BSc and B. Tech Students – Rs. 1180/- (Inclusive of 18% GST on Rs. 1000/-)
Payment	NEFT or IMPS Account Details: IIITDM Educational Events; Acc.No:35594334673; State Bank of India; Kandigai Branch; IFSC code: SBIN0018365. Please mail payment receipt to noor@iiitdm.ac.in, in order to Get Confirmation.
Contact Info:	Dr Noor Mahammad Sk, Organizing Chair (http://web.iiitdm.ac.in/noor/) Dr Ayesha Sk, Program Chair Indian Institute of Information Technology, Design and Manufacturing (IIITDM) Kancheepuram Melakottaiyur, Vandalur - Kelambakkam Road, Chennai - 600 127, Tamil Nadu, India. For enquiry and clarification, please contact: Email: noorse@gmail.com; 044-2747 6349/ 91760 10587(M)



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		Time (Hrs)	Topic	
DAY 1	6 DEC 2021	0930-1100	Introduction to HPC	Dr NMM
		1115-1230	Modern Processor Architectures – ILP to TLP	Dr NMM
		1400-1530	Introduction to Parallel Programming	Dr NMM
		1530-1700	Practice Session1: Profiling of Serial Code	Dr NMM
DAY 2	7 DEC 2021	0930-1100	Memory Access	Dr NMM
		1115-1230	Introduction to OpenMP	Dr NMM
		1400-1530	Practice Session2: Parallel Programming using OpenMP	Dr Ayesha VIT
		1530-1700	Practice Session3: OpenMP Data Races and Dead lock	Dr NMM
DAY 3	8 DEC 2021	0930-1100	Cluster and Distributed Computing Architectures	Dr Ayesha VIT
		1115-1230	Introduction to MPI Programming	Dr NMM
		1400-1530	Practice Session4: Parallel Programming using Collective Communication	Dr NMM
		1530-1700	Practice Session5: Parallel Programming using Collective Communication	Dr NMM
DAY 4	9 DEC 2021	0930-1100	Point to Point Communication using MPI, Data Races and Barrier Points	Dr NMM
		1115-1230	GPGPU Architectures	
		1400-1530	Practice Session6: Point to Point Communication using MPI	Dr NMM
		1530-1700	Practice Session7: Point to Point Communication using MPI	Dr NMM
DAY 5	10 DEC 2021	0930-1100	CUDA Programming Concepts	Dr NMM
		1115-1230	Practice Session8: CUDA Programming	Dr NMM
		1400-1530	Practice Session9: CUDA Programming	Dr Rama,IITTP
		1530-1700	Practice Session10: CUDA Programming	Dr Rama,IITTP