INDIAN INSTITUTE OF INFORMATION TECHNOLOGY
DESIGN AND MANUFACTURING (IIITD&M) KANCHEEPURAM

INTRODUCTION OF NEW COURSE

Course Title	Digital Systems Testing and Testable Design	Course No *(will be assigned)*				
Specialization	Computer Engineering	Structure (LTPC)	3	0	0	3
Offered for	UG/PG/Ph.D	Status	Core ☐		Elective ■	
Faculty	Dr Noor Mahammad Sk	Type	New ■		Modification ☐	
Pre-requisite	COT	To take effect from	Aug 2012			
Submission date	Jan 2012	Date of approval by AAC				
Objectives	The course aims at imparting skills required for the design of an efficient testable circuit and optimal test vectors to detect all possible detectable faults in a digital system. Broad areas of fault analysis, test generation and design for testability for digital integrated circuits and systems are discussed in depth.					
Contents of the course *(With approximate break up of hours)*	Design and Test, Test Concerns, HDLs in Digital System Test, ATE Architecture and Instrumentation - Using Verilog in Design, Using Verilog in Test, Basic Structures of Verilog, Combinational Circuits, Sequential Circuits, Testbench Techniques and PLI Basics - Fault Modeling, Structural Gate Level Faults, Issues Related to Gate Level Faults, Fault Collapsing and Fault Collapsing in Verilog - Fault Simulation, Fault Simulation Applications, Fault Simulation Technologies - Test Generation Basics, Controllability and Observability, Random Test Generation - Deterministic Test Generation Methods, Sequential Circuit Test Generation, Test Data Compaction - Making Circuits Testable, Testability Insertion, Full Scan DFT Technique, Scan Architectures and RT Level Scan Design - Boundary Scan Basics, Boundary Scan Architecture, Boundary Scan Test Instructions, Board Level Scan Chain Structure, RT Level Boundary Scan and Boundary Scan Description Language - Logic Built-in Self-test: BIST Basics, Test Pattern Generation, Output Response Analysis, BIST Architectures, RT Level BIST Design Test Data Compression, Compression Methods and Decompression Methods Memory Testing, Memory Structure, Memory Fault Model, Functional Test Procedures and MBIST Methods.					
Textbook	1. M. Abramovici, M. A. Breuer and A. D. Friedman, Digital Systems Testing and Testable Design, Wiley-IEEE Press, 1st Edition, 1994.					
References	2. Zainalabedin Navabi, Digital System Test and Testable Design Using HDL Models and Architectures, Springer, 1st Edition, December 2010. 3. Niraj K. Jha, Sandeep Gupta, Testing of Digital Systems, Cambridge University Press, 1st Edition, 2003. 4. M. L. Bushnell and V. D. Agrawal, Essentials of Electronic Testing, Kluwer Academic Publishers, 1st Edition, 2004.					